Chettinad College of Engineering & Technology
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai.

Department of Electronics and Communication Engineering

EC8095 – VLSI DESIGN

Unit I - MCQ Bank

1.The difficulty in achieving high doping concentration leads to _____

a) Error in concentration

b) Error in variation

c) Error in doping

d) Distribution error

Answer: b

2. As die size shrinks, the complexity of making the photomasks _____

a) Increases

b) Decreases

c) Remains the same

d) Cannot be determined

Answer: a

3.What is the design flow of VLSI system?

i. Architecture design

ii. Market requirement

iii. Logic design

iv. HDL coding

a) ii-i-iii-iv

b) iv-i-iii-ii

c) iii-ii-i-iv

d) i-ii-iii-iv

Answer: a

4. Pass transistor can be driven through _____ pass transistors.

a) One

b) No

c) More

d) Two

Answer: b

5. When one pass transistor is driven using another, threshold voltage ----------

a) Affects

b) Does not affect

c) All of the mentioned

d) None of the mentioned

Answer: a

6. The condition for non saturated region is

a) Vds = Vgs – Vt

b) Vgs lesser than Vt

c) Vds lesser than Vgs – Vt

d) Vds greater than Vgs – Vt

Answer: c

7. In enhancement mode, device is in condition ----------

a) Conducting

b) Non conducting

c) Partially conducting

d) Insulating

Answer: b

8. The condition for non conducting mode is ----------

a) Vds lesser than Vgs

b) Vgs lesser than Vds

c) Vgs = Vds = 0

d) Vgs = Vds = Vs = 0

Answer: d

9. The condition for linear region is ----------

a) Vgs lesser than Vt

b) Vgs greater than Vt

c) Vds lesser than Vgs

d) Vds greater than Vgs

Answer: b

10. MOS transistors consists of ----------

a) Semiconductor layer

b) Metal layer

c) Layer of silicon-di-oxide

d) All of the mentioned

Answer: d

11. The gate region consists of ----------

a) Insulating layer

b) Conducting layer

c) Lower metal layer

d) P type layer

Answer: b

12. In N channel MOSFET which is the more negative of the elements?

a) Source

b) Gate

c) Drain

d) Source and Drain

Answer: a

13. If the gate is given sufficiently large charge, electrons will be attracted to ----------

a) Drain region

b) Channel region

c) Switch region

d) Bulk region

Answer: b

14. Threshold voltage is negative for ----------

a) nMOS depletion

b) nMOS enhancement

c) pMOS depletion

d) pMOS enhancement

Answer: a

15. When the channel pinches off?

a) Vgs>Vds

b) Vds>Vgs

c) Vds>(Vgs-Vth)

d) Vgs>(Vds-Vth)

Answer: c

16. Stick diagrams are those which convey layer information through ----------

a) Thickness

b) Color

c) Shapes

d) Layers

Answer: b

17. Stick diagram gives the position of placement of the element.

a) True

b) False

Answer: b

18. Circuit design concepts can also be represented using symbolic diagram.

a) True

b) False

Answer: a

19. The width of n-diffusion and p-diffusion layer should be ----------

a) 3λ

b) 2λ

c) λ

d) 4λ

Answer: b

20. The overall delay of nMOS inverter pair is ----------

a) 4τ

b) τ

c) 5τ

d) 2τ

Answer: c

21. The assymetry of resistance value can be eliminated by ----------

a) Decreasing the width

b) Increasing the width

c) Increasing the length

d) Increasing the width

Answer: b

22. The saturation current is scaled by the factor of ----------

a) 1

b) $1/\alpha^2$

c) 1/β

d) $1/\alpha$

Answer: c

23. In Constant field model, the scaling factor of switching energy per gate would be ----------:

a) $1/ \beta.\alpha^2$

b) $1/ \alpha^3$

c) $1/ \alpha^2$

d) All of the mentioned

Answer: b

24. The maximum operating frequency is scaled by ----------:

a) $1/\alpha^2$

b) β/α^2

c) α^2/β

d) 1

Answer: c

25. Which gives scalable design rules?

a) Lambda rules

b) Micron rules

c) layer rules

d) Thickness rules

Answer: a